

MEMORY

**CMOS 4M × 4 BIT
HYPER PAGE DYNAMIC RAM****MB8116405A-60/-70****CMOS 4,194,304 × 4 BIT Hyper Page Mode Dynamic RAM****DESCRIPTION**

The Fujitsu MB8116405A is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 4-bit increments. The MB8116405A features a "hyper page" mode of operation whereby high-speed random access of up to 1,024-bits of data within the same row can be selected. The MB8116405A DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB8116405A is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB8116405A is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon and two-layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB8116405A are not critical and all inputs are TTL compatible.

ABSOLUTE MAXIMUM RATINGS (See Note.)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +7	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +7	V
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OUT}	-50 to +50	mA
Operating Temperature	T_{OPE}	0 to 70	°C
Storage Temperature	T_{STG}	-55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

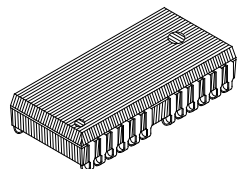
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■ PRODUCT LINE & FEATURES

Parameter		MB8116405A-60	MB8116405A-70
RAS Access Time		60 ns max.	70 ns max.
Random Cycle Time		104 ns min.	124 ns min.
Address Access Time		30 ns max.	35 ns max.
CAS Access Time		15 ns max.	17 ns max.
Hyper Page Mode Cycle Time		25 ns min.	30 ns min.
Low power Dissipation	Operating current	412.5 mW max.	357.5 mW max.
	Standby current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)	

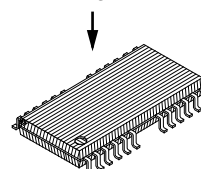
- 4,194,304 words × 4 bit organization
- Silicon gate, CMOS, Advanced Capacitor Cell
- All input and output are TTL compatible
- 4096 refresh cycles every 65.6 ms
- Early Write or OE controlled write capability
- RAS only, CAS-before-RAS, or Hidden Refresh
- Hyper Page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

■ PACKAGE



Plastic SOJ Package
(LCC-26P-M09)

Marking side



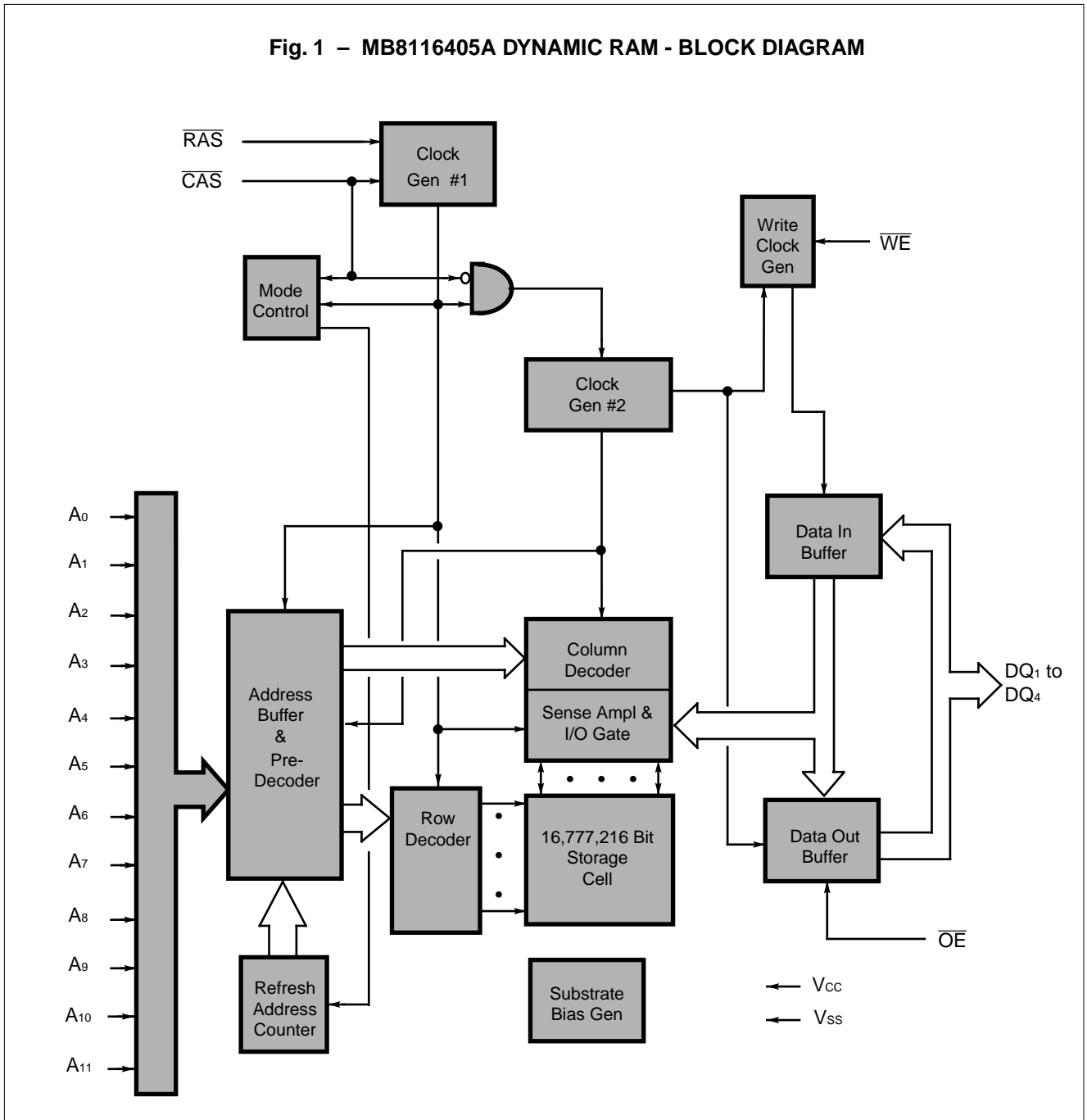
Plastic TSOP Packages
(FPT-26P-M05)

Package and Ordering Information

- 26-pin plastic (300 mil) SOJ, order as MB8116405A-xxPJ
- 26-pin plastic (300 mil) TSOP-II with normal bend leads, order as MB8116405A-xxPFTN

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Fig. 1 - MB8116405A DYNAMIC RAM - BLOCK DIAGRAM



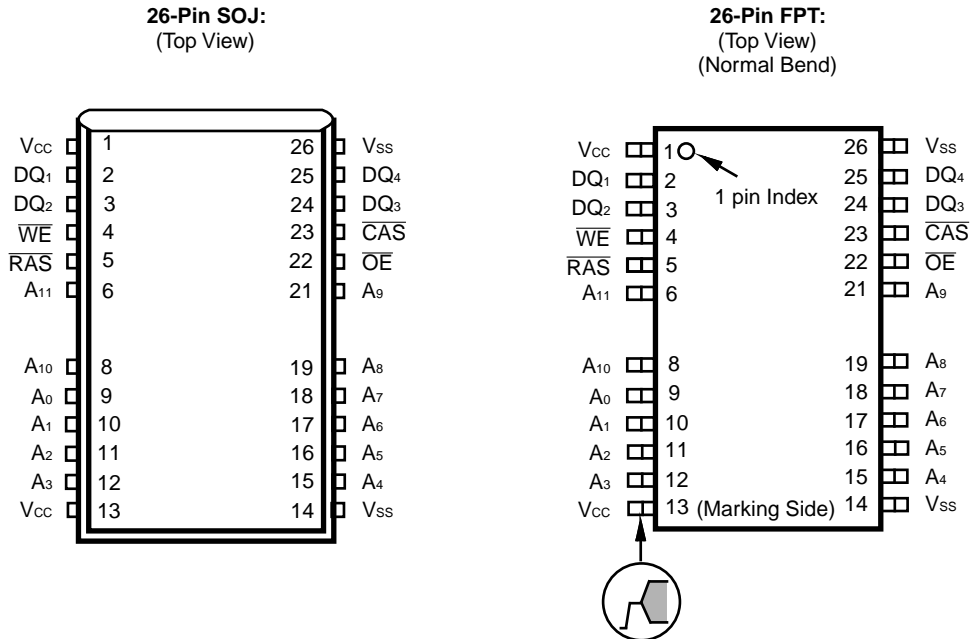
■ CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A ₀ to A ₁₁	C _{IN1}	—	5	pF
Input Capacitance, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	C _{IN2}	—	5	pF
Input/Output Capacitance, DQ ₁ to DQ ₄	C _{IN3}	—	7	pF

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■ PIN ASSIGNMENTS AND DESCRIPTIONS



Designator	Function
DQ ₀ to DQ ₄	Data Input/Output
\overline{WE}	Write Enable.
\overline{RAS}	Row address strobe.
A ₀ to A ₁₁	Address inputs.
V _{CC}	+5 volt power supply.
\overline{OE}	Output enable.
\overline{CAS}	Column address strobe.
V _{SS}	Circuit ground.

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■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp.
Supply Voltage	1	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
		V_{SS}	0	0	0		
Input High Voltage, All Inputs	1	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, All Inputs/Outputs*	1	V_{IL}	-0.3	—	0.8	V	

* : Undershoots of up to -2.0 volts with a pulse width not exceeding 20 ns are acceptable.

■ FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty-two input bits are required to decode any four of 16,777,216 cell addresses in the memory matrix. Since only twelve address bits (A_0 to A_{11}) are available, the row and column inputs are separately strobed by \overline{RAS} and \overline{CAS} as shown in Figure 1. First, twelve row address bits are input on pins A_0 -through- A_{11} and latched with the row address strobe (\overline{RAS}) then, ten column address bits are input and latched with the column address strobe (\overline{CAS}). Both row and column addresses must be stable on or before the falling edge of \overline{RAS} and \overline{CAS} , respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min.) + tT is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of \overline{WE} . When \overline{WE} is active Low, a write cycle is initiated; when \overline{WE} is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUT

Input data is written into memory in either of three basic ways : an early write cycle, an \overline{OE} (delayed) write cycle, and a read-modify-write cycle. The falling edge of \overline{WE} or \overline{CAS} , whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data (DQ_1 to DQ_4) is strobed by \overline{CAS} and the setup/hold times are referenced to \overline{CAS} because \overline{WE} goes Low before \overline{CAS} . In a delayed write or a read-modify-write cycle, \overline{WE} goes Low after \overline{CAS} ; thus, input data is strobed by \overline{WE} and all setup/hold times are referenced to the write-enable signal.

DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs and High-Z state are obtained under the following conditions:

- t_{RAC} : from the falling edge of \overline{RAS} when t_{RCD} (max.) is satisfied.
- t_{CAC} : from the falling edge of \overline{CAS} when t_{RCD} is greater than t_{RCD} (max.).
- t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max.), and t_{RCD} (max.) is satisfied.
- t_{OEA} : from the falling edge of \overline{OE} when \overline{OE} is brought Low after t_{RAC} , t_{CAC} , or t_{AA} .
- t_{OEZ} : from \overline{OE} inactive.
- t_{OFF} : from \overline{CAS} inactive while \overline{RAS} inactive.
- t_{OFR} : from \overline{RAS} inactive while \overline{CAS} inactive.
- t_{WEZ} : from \overline{WE} active while \overline{CAS} inactive.

The data remains valid after either \overline{OE} is inactive, or both \overline{RAS} and \overline{CAS} are inactive, or \overline{CAS} is reactivated. When an early write is execute, the output buffers remain in a high-impedance state during the entire cycle.

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HYPER PAGE MODE OPERATION

The hyper page mode of operation provides faster memory access and lower power dissipation. The hyper page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{\text{RAS}}$ is held Low for all contiguous memory cycles in which row addresses are common. For each page of memory (with $\overline{\text{column}}$ address locations), any of 1,024-bits can be accessed and, when multiple MB8116405As are used, $\overline{\text{CAS}}$ is decoded to select the desired memory page. Hyper page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted. Hyper page mode features that output remains valid when $\overline{\text{CAS}}$ is inactive until $\overline{\text{CAS}}$ is reactivated.

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■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Note 3

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min.	Typ.	Max.	
Output High Voltage	1	V_{OH}	$I_{OH} = -5 \text{ mA}$	2.4	—	—	V
Output Low Voltage	1	V_{OL}	$I_{OL} = 4.2 \text{ mA}$	—	—	0.4	
Input Leakage Current (Any Input)		$I_{I(L)}$	$0 \text{ V} \leq V_{IN} \leq 5.5 \text{ V};$ $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V};$ $V_{SS} = 0 \text{ V};$ All other pins under test = 0 V	-10	—	10	μA
Output Leakage Current		$I_{O(L)}$	$0 \text{ V} \leq V_{OUT} \leq 5.5 \text{ V};$ Data out disabled	-10	—	10	
Operating Current (Average Power Supply Current) 2	MB8116405A-60	I_{CC1}	$\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ cycling; $t_{RC} = \text{min.}$	—	—	75	mA
	MB8116405A-70					65	
Standby Current (Power Supply Current)	TTL level	I_{CC2}	$\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$	—	—	2.0	mA
	CMOS level		$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2$			1.0	
Refresh Current#1 (Average Power Supply Current) 2	MB8116405A-60	I_{CC3}	$\overline{\text{CAS}} = V_{IH}, \overline{\text{RAS}}$ cycling; $t_{RC} = \text{min.}$	—	—	75	mA
	MB8116405A-70					65	
Fast Page Mode Current 2	MB8116405A-60	I_{CC4}	$\overline{\text{RAS}} = V_{IL}, \overline{\text{CAS}}$ cycling; $t_{HPC} = \text{min.}$	—	—	75	mA
	MB8116405A-70					65	
Refresh Current#2 (Average Power Supply Current) 2	MB8116405A-60	I_{CC5}	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$; $t_{RC} = \text{min.}$	—	—	75	mA
	MB8116405A-70					65	

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■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB8116405A-60		MB8116405A-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t _{REF}	—	65.6	—	65.6	ms
2	Random Read/Write Cycle Time		t _{RC}	104	—	124	—	ns
3	Read-Modify-Write Cycle Time		t _{RWC}	138	—	162	—	ns
4	Access Time from $\overline{\text{RAS}}$	6, 9	t _{RAC}	—	60	—	70	ns
5	Access Time from $\overline{\text{CAS}}$	7, 9	t _{CAC}	—	15	—	17	ns
6	Column Address Access Time	8, 9	t _{AA}	—	30	—	35	ns
7	Output Hold Time		t _{OH}	3	—	3	—	ns
8	Output Hold Time from $\overline{\text{CAS}}$		t _{OHc}	5	—	5	—	ns
9	Output Buffer Turn On Delay Time		t _{ON}	0	—	0	—	ns
10	Output Buffer Turn Off Delay Time	10	t _{OFF}	—	15	—	17	ns
11	Output Buffer Turn Off Delay Time from $\overline{\text{RAS}}$	10	t _{OFFR}	—	15	—	17	ns
12	Output Buffer Turn Off Delay Time from $\overline{\text{WE}}$	10	t _{WEZ}	—	15	—	17	ns
13	Transition Time		t _T	1	50	1	50	ns
14	$\overline{\text{RAS}}$ Precharge Time		t _{RP}	40	—	50	—	ns
15	$\overline{\text{RAS}}$ Pulse Width		t _{RAS}	60	100000	70	100000	ns
16	$\overline{\text{RAS}}$ Hold Time		t _{RSH}	15	—	17	—	ns
17	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	21	t _{CRP}	5	—	5	—	ns
18	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	11, 12, 22	t _{RCD}	14	45	14	53	ns
19	$\overline{\text{CAS}}$ Pulse Width		t _{CAS}	10	—	13	—	ns
20	$\overline{\text{CAS}}$ Hold Time		t _{CSH}	40	—	50	—	ns
21	$\overline{\text{CAS}}$ Precharge Time (Normal)	19	t _{CPN}	10	—	10	—	ns
22	Row Address Set Up Time		t _{ASR}	0	—	0	—	ns
23	Row Address Hold Time		t _{RAH}	10	—	10	—	ns
24	Column Address Set Up Time		t _{ASC}	0	—	0	—	ns
25	Column Address Hold Time		t _{CAH}	10	—	10	—	ns
26	Column Address Hold Time from $\overline{\text{RAS}}$		t _{AR}	24	—	24	—	ns
27	$\overline{\text{RAS}}$ to Column Address Delay Time	13	t _{RAD}	12	30	12	35	ns
28	Column Address to $\overline{\text{RAS}}$ Lead Time		t _{RAL}	30	—	35	—	ns
29	Column Address to $\overline{\text{CAS}}$ Lead Time		t _{CAL}	23	—	28	—	ns
30	Read Command Set Up Time		t _{RCS}	0	—	0	—	ns
31	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	14	t _{RRH}	0	—	0	—	ns
32	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	14	t _{RCH}	0	—	0	—	ns
33	Write Command Set Up Time	15, 20	t _{WCS}	0	—	0	—	ns
34	Write Command Hold Time		t _{WCH}	10	—	10	—	ns

(Continued)

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■ AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.)

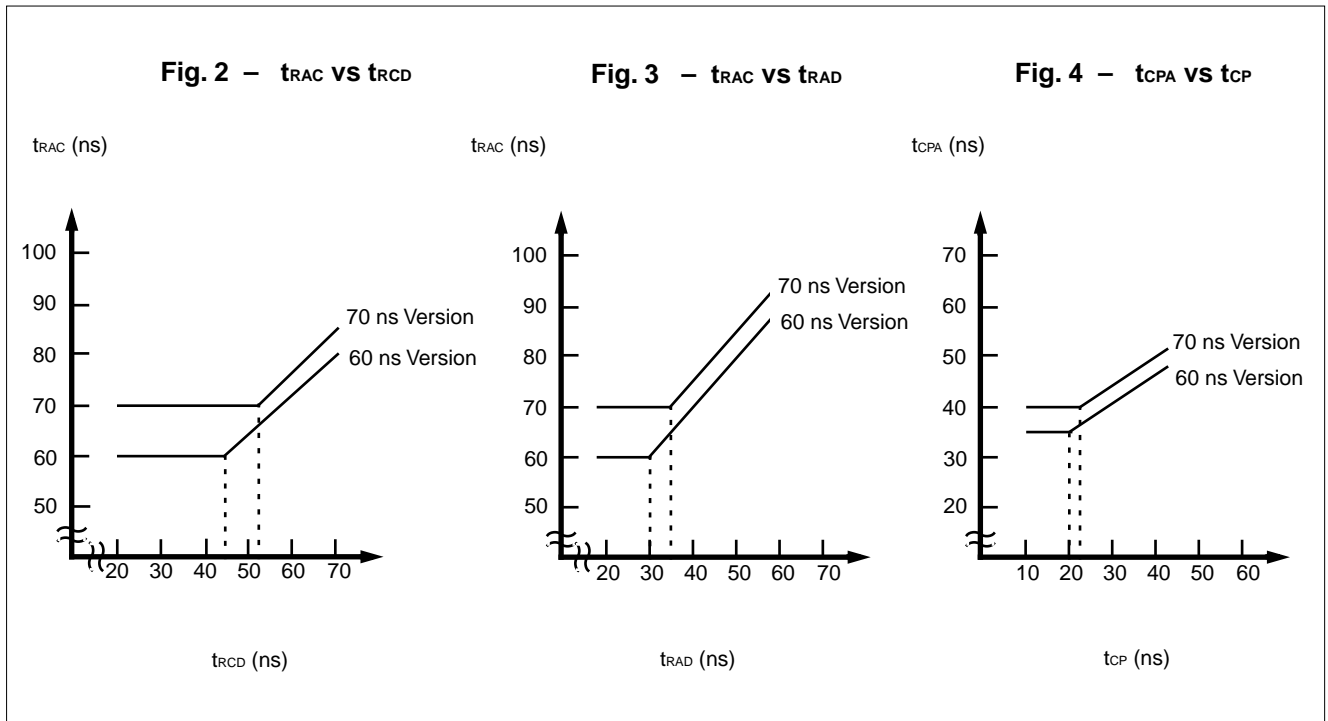
Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB8116405A-60		MB8116405A-70		Unit
				Min.	Max.	Min.	Max.	
35	Write Hold Time from $\overline{\text{RAS}}$		t_{WCR}	24	—	24	—	ns
36	$\overline{\text{WE}}$ Pulse Width		t_{WP}	10	—	10	—	ns
37	Write Command to $\overline{\text{RAS}}$ Lead Time		t_{RWL}	15	—	17	—	ns
38	Write Command to $\overline{\text{CAS}}$ Lead Time		t_{CWL}	10	—	13	—	ns
39	DIN Set Up Time		t_{DS}	0	—	0	—	ns
40	DIN Hold Time		t_{DH}	10	—	10	—	ns
41	Data Hold Time from $\overline{\text{RAS}}$		t_{DHR}	24	—	24	—	ns
42	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	20	t_{RWD}	77	—	89	—	ns
43	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	20	t_{CWD}	32	—	36	—	ns
44	Column Address to $\overline{\text{WE}}$ Delay Time	20	t_{AWD}	47	—	54	—	ns
45	$\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active Time (Refresh cycles)		t_{RPC}	5	—	5	—	ns
46	$\overline{\text{CAS}}$ Set Up Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh		t_{CSR}	0	—	0	—	ns
47	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh		t_{CHR}	10	—	12	—	ns
48	Access time from $\overline{\text{OE}}$	9	t_{OEA}	—	15	—	17	ns
49	Output Buffer Turn Off Delay from $\overline{\text{OE}}$	10	t_{OEZ}	—	15	—	17	ns
50	$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	ns
51	$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ Lead Time		t_{COL}	5	—	5	—	ns
52	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{WE}}$	16	t_{OEH}	5	—	5	—	ns
53	$\overline{\text{OE}}$ to Data in Delay Time		t_{OED}	15	—	17	—	ns
54	$\overline{\text{RAS}}$ to Data in Delay Time		t_{RDD}	15	—	17	—	ns
55	$\overline{\text{CAS}}$ to Data in Delay Time		t_{CDD}	15	—	17	—	ns
56	DIN to $\overline{\text{CAS}}$ Delay Time	17	t_{DZC}	0	—	0	—	ns
57	DIN to $\overline{\text{OE}}$ Delay Time	17	t_{DZO}	0	—	0	—	ns
58	$\overline{\text{OE}}$ Precharge Time		t_{OEP}	8	—	8	—	ns
59	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{CAS}}$		t_{OECH}	10	—	10	—	ns
60	$\overline{\text{WE}}$ Precharge Time		t_{WPZ}	8	—	8	—	ns
61	$\overline{\text{WE}}$ to Date In Delay Time		t_{WED}	15	—	17	—	ns
62	Hyper Page Mode $\overline{\text{RAS}}$ Pulse width		t_{RASP}	—	100000	—	100000	ns
63	Hyper Page Mode Read/Write Cycle Time		t_{HPC}	25	—	30	—	ns
64	Hyper Page Mode Read-Modify-Write Cycle Time		t_{HPRWC}	69	—	79	—	ns
65	Access Time from $\overline{\text{CAS}}$ Precharge	9, 18	t_{CPA}	—	35	—	40	ns
66	Hyper Page Mode $\overline{\text{CAS}}$ Precharge Time		t_{CP}	10	—	10	—	ns
67	Hyper Page Mode $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge		t_{RHCP}	35	—	40	—	ns
68	Hyper Page Mode $\overline{\text{CAS}}$ Precharge to $\overline{\text{WE}}$ Delay Time		t_{CPWD}	52	—	59	—	ns

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- Notes:
1. Referenced to V_{SS} .
 2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open. I_{CC} depends on the number of address change as $\overline{RAS} = V_{IL}$, $\overline{CAS} = V_{IH}$ and $V_{IL} > -0.3 V$. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$. I_{CC2} is specified during $\overline{RAS} = V_{IH}$ and $V_{IL} > -0.3 V$.
 3. An initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 μs is required after power-up followed by any eight \overline{RAS} -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight \overline{CAS} -before- \overline{RAS} initialization cycles instead of 8 \overline{RAS} cycles are required.
 4. AC characteristics assume $t_T = 2 ns$.
 5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min.) and V_{IL} (max.).
 6. Assumes that $t_{RCD} \leq t_{RCD} (max.)$, $t_{RAD} \leq t_{RAD} (max.)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
 7. If $t_{RCD} \geq t_{RCD} (max.)$, $t_{RAD} \geq t_{RAD} (max.)$, and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC} .
 8. If $t_{RAD} \geq t_{RAD} (max.)$ and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA} .
 9. Measured with a load equivalent to two TTL loads and 50 pF.
 10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.
 11. Operation within the $t_{RCD} (max.)$ limit ensures that $t_{RAC} (max.)$ can be met. $t_{RCD} (max.)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD} (max.)$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 12. $t_{RAD} (min.) = t_{RAH} (min.) + 2 t_T + t_{ASC} (min.)$.
 13. Operation within the $t_{RAD} (max.)$ limit ensures that $t_{RAC} (max.)$ can be met. $t_{RAD} (max.)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD} (max.)$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
 15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS} (min.)$ the data output pin will remain High-Z state through entire cycle.
 16. Assumes that $t_{WCS} < t_{WCS} (min.)$.
 17. Either t_{DZC} or t_{DZO} must be satisfied.
 18. t_{CPA} is access time from the selection of a new column address (that is caused by changing \overline{CAS} from "L" to "H"). Therefore, if t_{OP} is long, t_{OPA} is longer than $t_{OPA} (max.)$.
 19. Assumes that \overline{CAS} -before- \overline{RAS} refresh.
 20. t_{WCS} , t_{CWD} , t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} > t_{WCS} (min.)$, the cycle is an early write cycle and D_{out} pin will maintain high impedance state throughout the entire cycle. If $t_{CWD} > t_{CWD} (min.)$, $t_{RWD} > t_{RWD} (min.)$, and $t_{AWD} > t_{AWD} (min.)$, the cycle is a read modify-write cycle and data from the selected cell will appear at the D_{out} pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the D_{out} pin, and write operation can be executed by satisfying t_{RWL} , t_{CWL} , and t_{RAL} specifications.
 21. The last \overline{CAS} rising edge.
 22. The first \overline{CAS} falling edge.

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FUNCTIONAL TRUTH TABLE

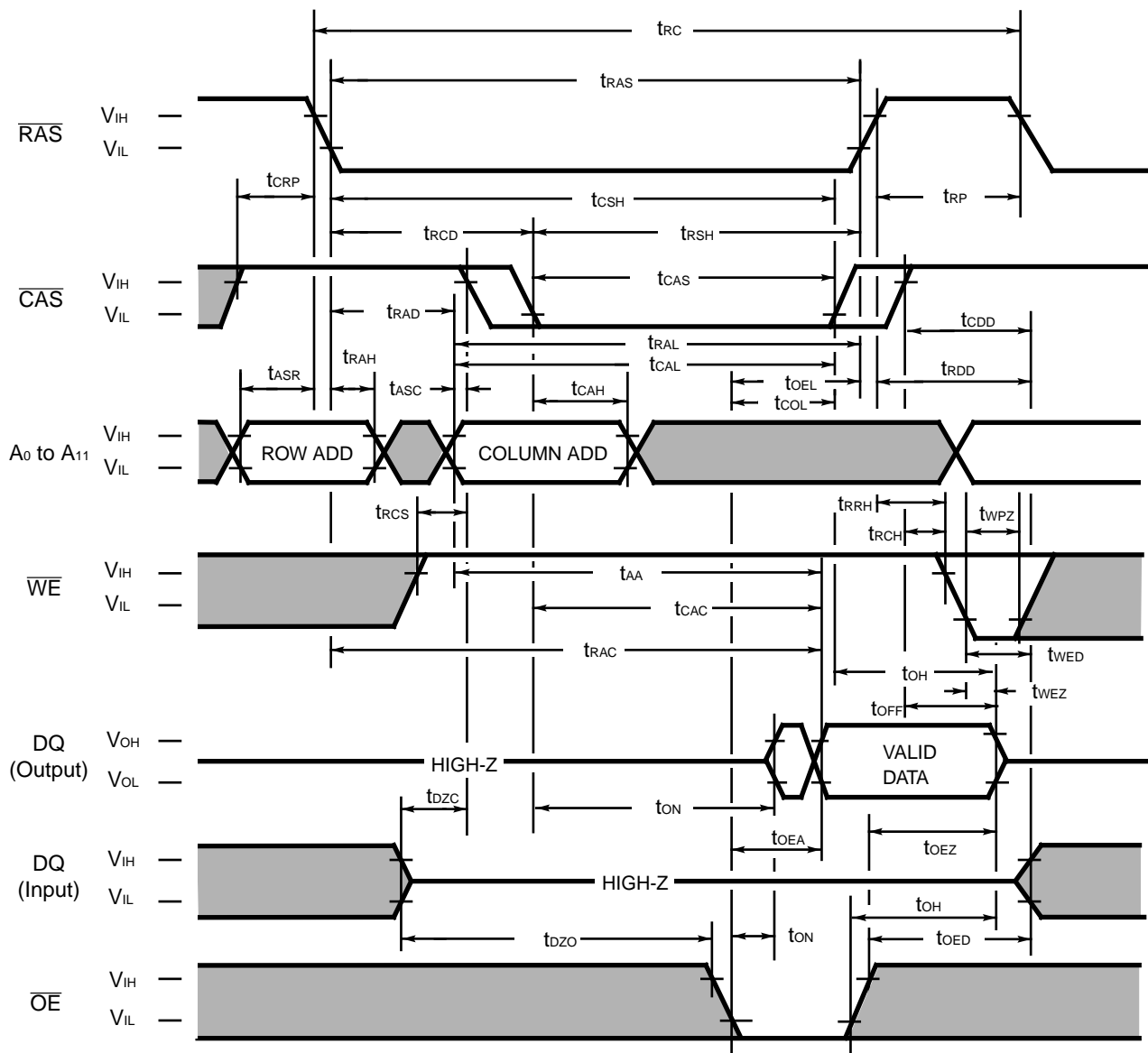
Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Row	Column	Input	Output		
Standby	H	H	X	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	L	Valid	—	—	Valid	Yes*	t _{RCS} ≥ t _{RCS} (min.)
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	Yes*	t _{WCS} ≥ t _{WCS} (min.)
Read-Modify-Write Cycle	L	L	H→L	H→L	Valid	Valid	Valid	Valid	Yes*	
$\overline{\text{RAS}}$ -only Refresh Cycle	L	H	X	X	Valid	—	—	High-Z	Yes	
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle	L	L	H	X	—	—	—	High-Z	Yes	t _{CSR} ≥ t _{CSR} (min.)
Hidden Refresh Cycle	H→L	L	H→X	L	—	—	—	High-Z	Yes	Previous data is kept.

X; "H" or "L"

*; It is impossible in Hyper Page Mode.

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Fig. 4 - READ CYCLE



DESCRIPTION

To implement a read operation, a valid address is latched in by the \overline{RAS} and \overline{CAS} and with \overline{WE} set to a High level and \overline{OE} set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by \overline{RAS} (t_{RAC}), \overline{CAS} (t_{CAC}), \overline{OE} (t_{OEA}) or column addresses (t_{AA}) under the following conditions:

If $t_{RCD} > t_{RCD}(\text{max.})$, access time = t_{CAC} .

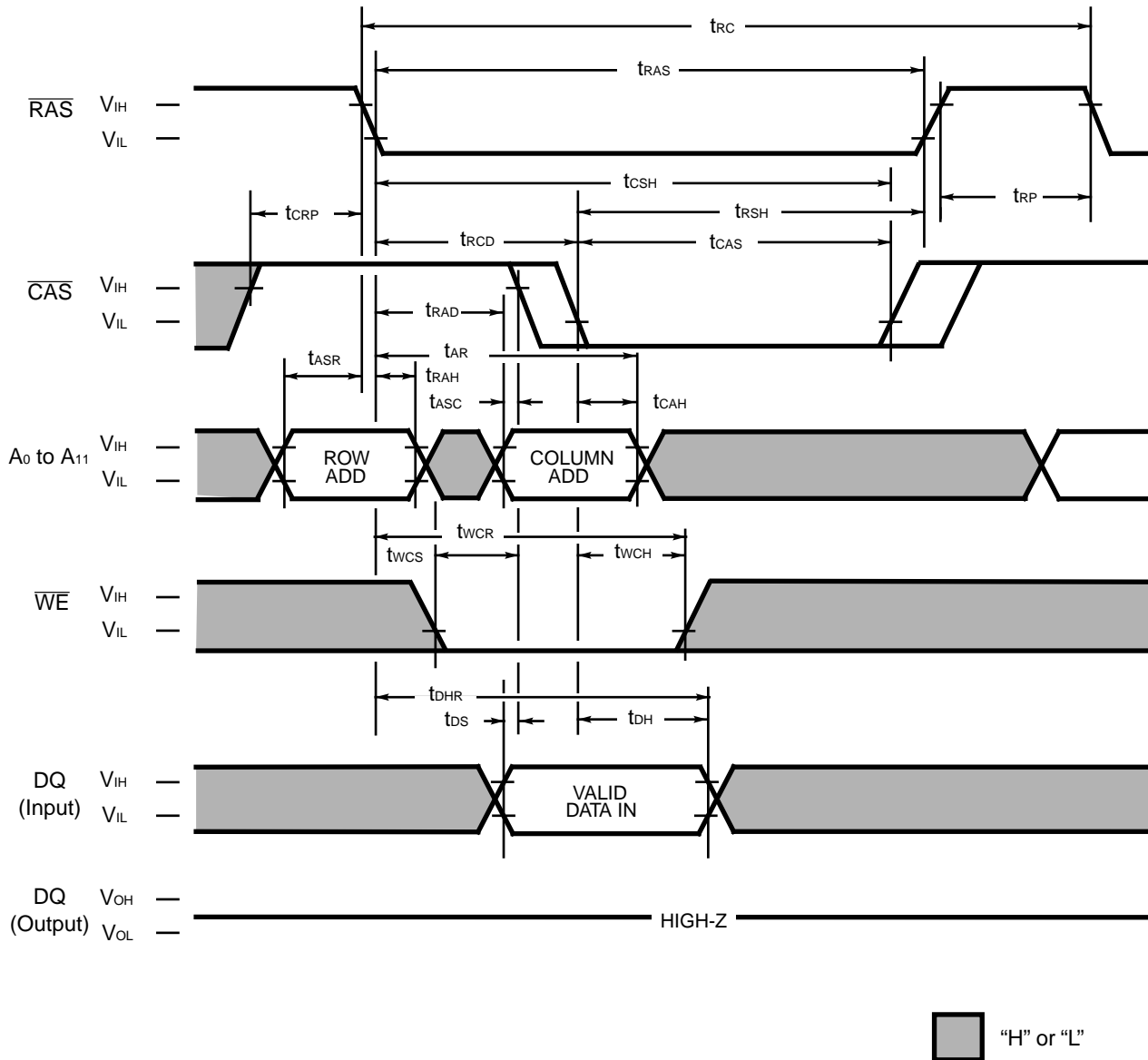
If $t_{RAD} > t_{RAD}(\text{max.})$, access time = t_{AA} .

If \overline{OE} is brought Low after t_{RAC} , t_{CAC} , or t_{AA} (whichever occurs later), access time = t_{OEA} .

However, if either CAS or OE goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

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Fig. 5 - EARLY WRITE CYCLE (\overline{OE} = "H" or "L")

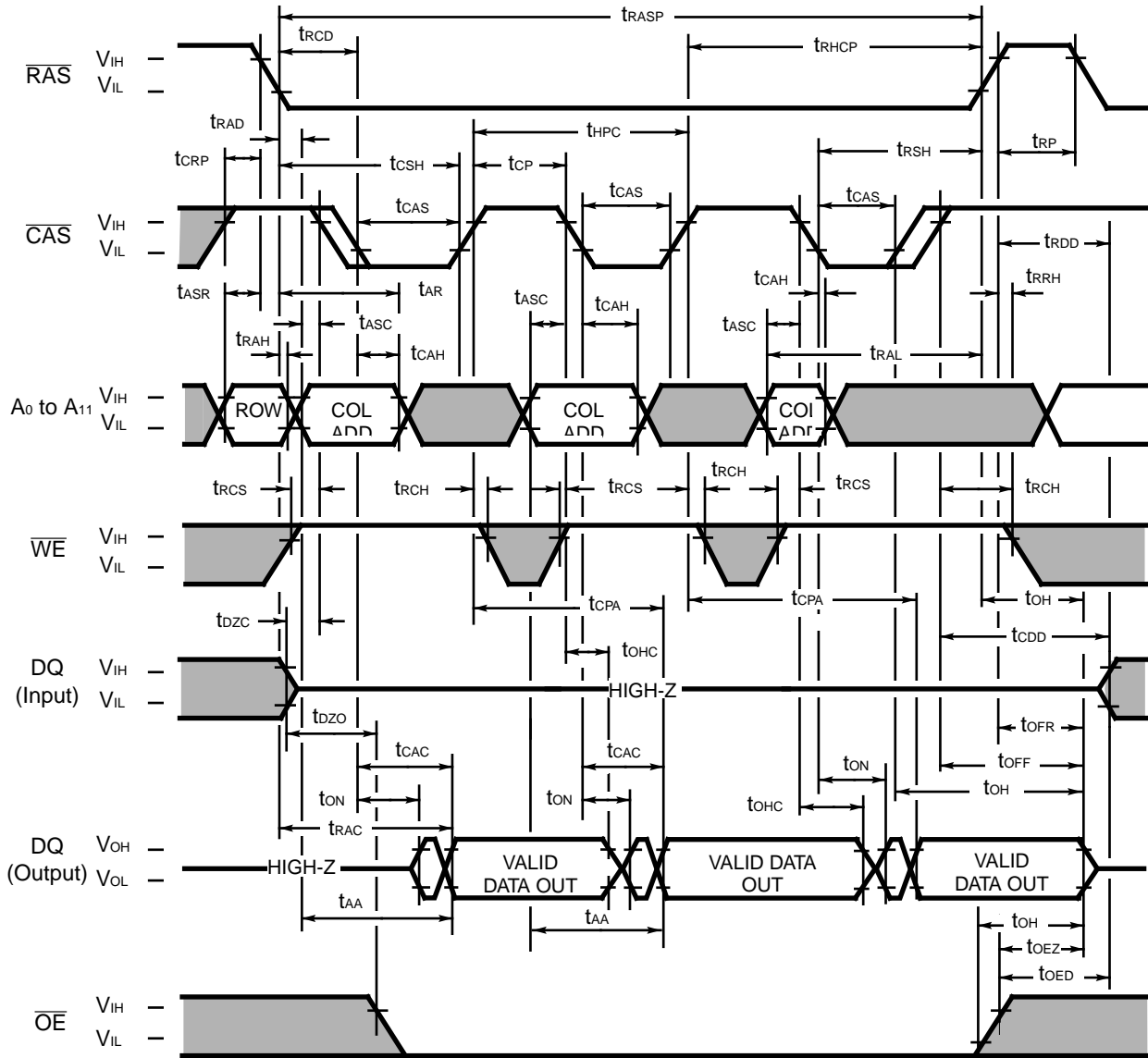


DESCRIPTION

A write cycle is similar to a read cycle except \overline{WE} is set to a Low state and \overline{OE} is a "H" or "L" signal. A write cycle can be implemented in either of three ways—early write, \overline{OE} write (delayed write), or read-modify-write. During all write cycles, timing parameters t_{RWL} , t_{CWL} and t_{RAL} must be satisfied. In the early write cycle shown above t_{WCS} is satisfied, data on the DQ pin is latched with the falling edge of \overline{CAS} and written into memory.

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Fig. 8 - HYPER PAGE MODE READ CYCLE



During one cycle is achieved in hyper-page mode, the input/output timing apply the same manner as the former cycle.

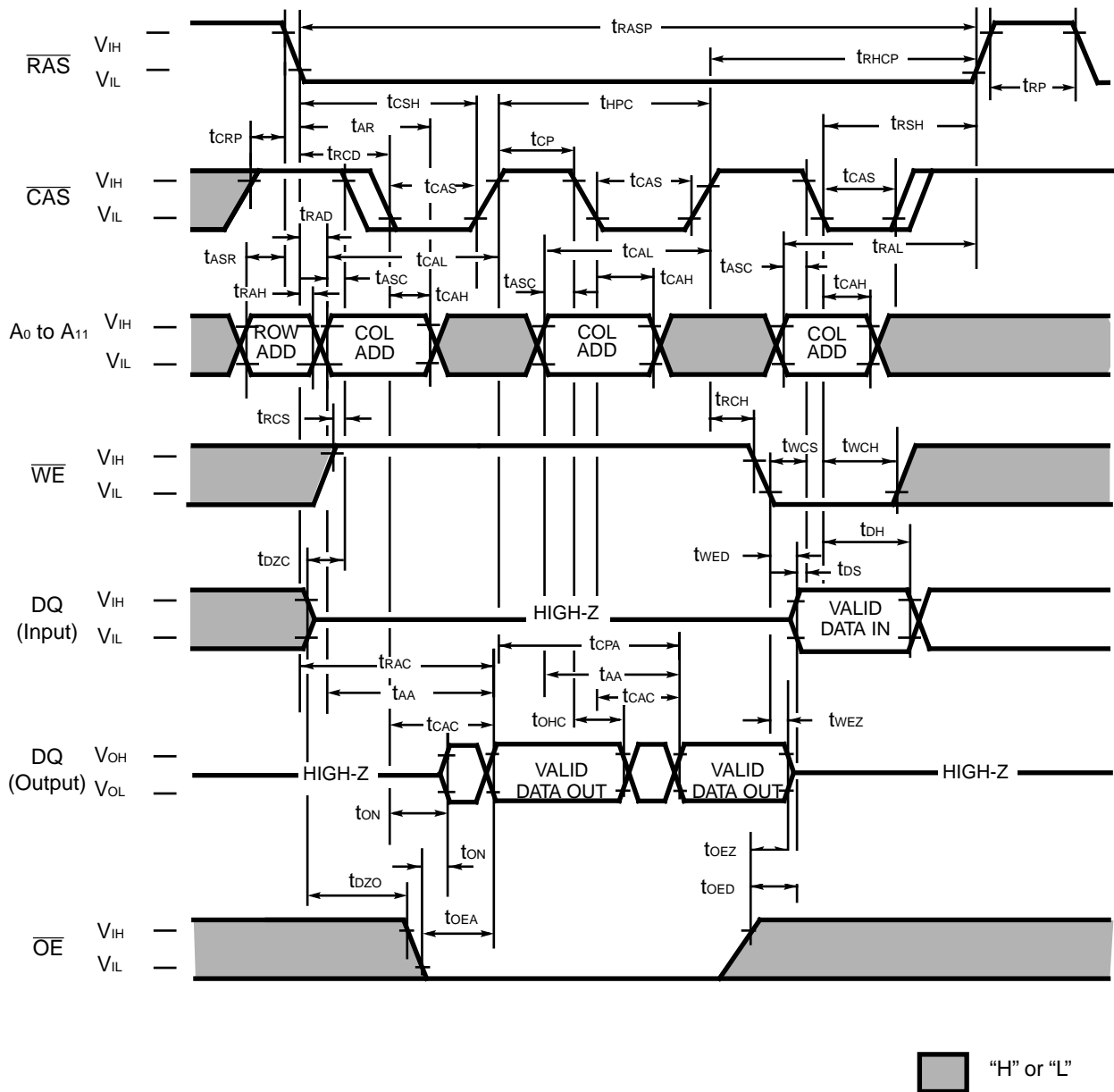
■ "H" or "L"

DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining RAS at a Low level during all successive memory cycles in which the row address is latched. The access time is determined by t_{CAC} , t_{AA} , t_{CPA} , or t_{OEA} , whichever one is the latest in occurring.

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Fig. 13 - HYPER PAGE MODE READ-WRITE CYCLE

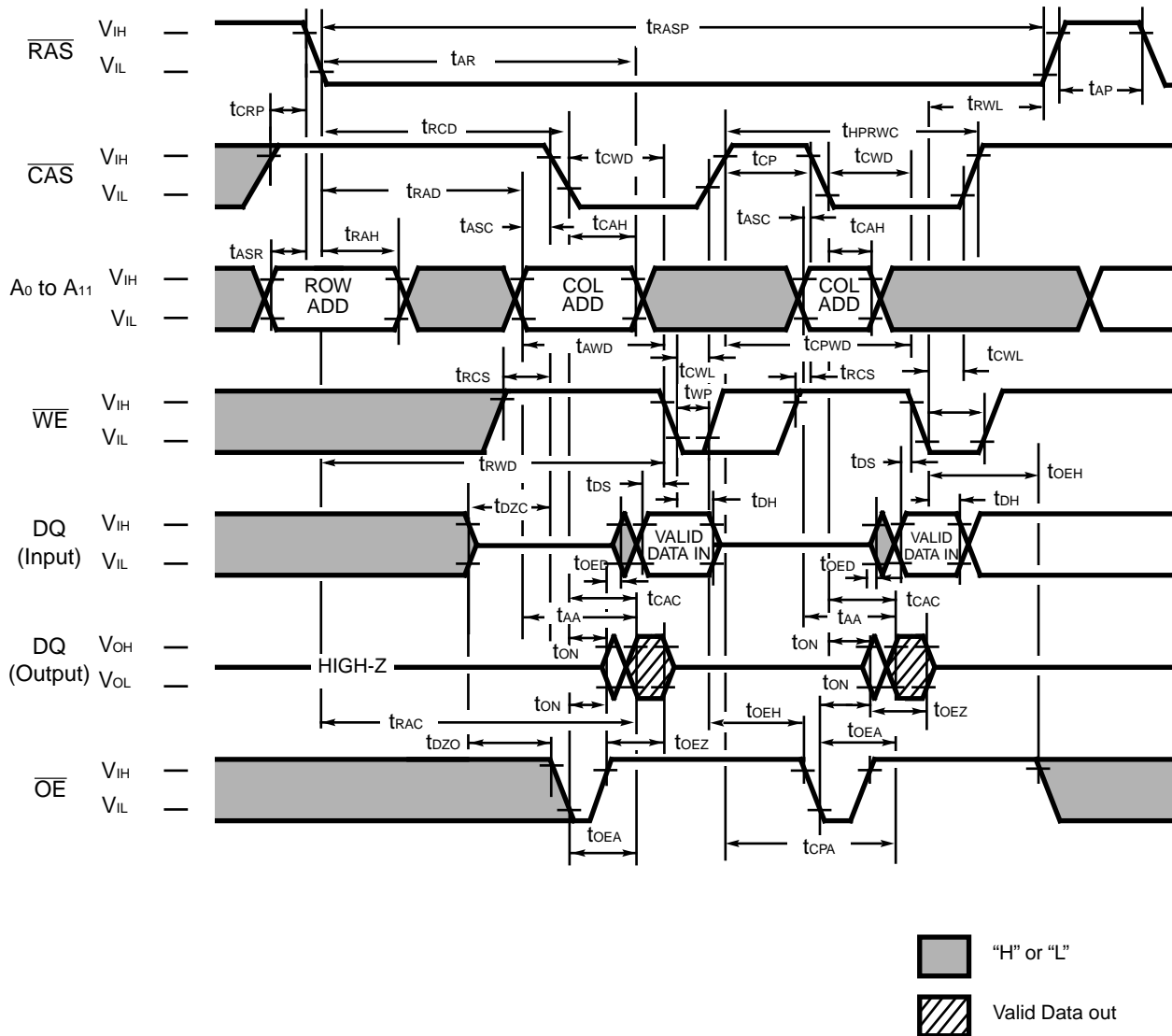


DESCRIPTION

The hyper page mode performs read/write operations repetitively during one \overline{RAS} cycle. At this time, t_{HPC} (min.) is invalid.

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Fig. 14 - HYPER PAGE MODE READ-MODIFY-WRITE CYCLE

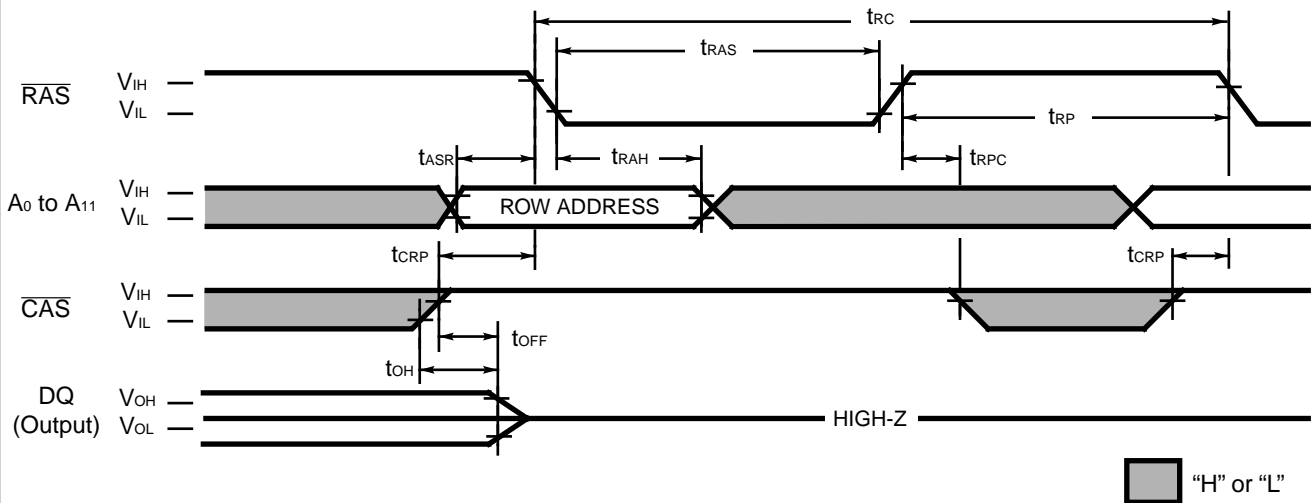


DESCRIPTION

During the hyper page mode of operation, the read-modify-write cycle can be executed by switching \overline{WE} from High to Low after input data appears at the DQ pins during a normal cycle.

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Fig. 15 - $\overline{\text{RAS}}$ -ONLY REFRESH ($\overline{\text{WE}} = \overline{\text{OE}} = \text{"H"}$ or "L")

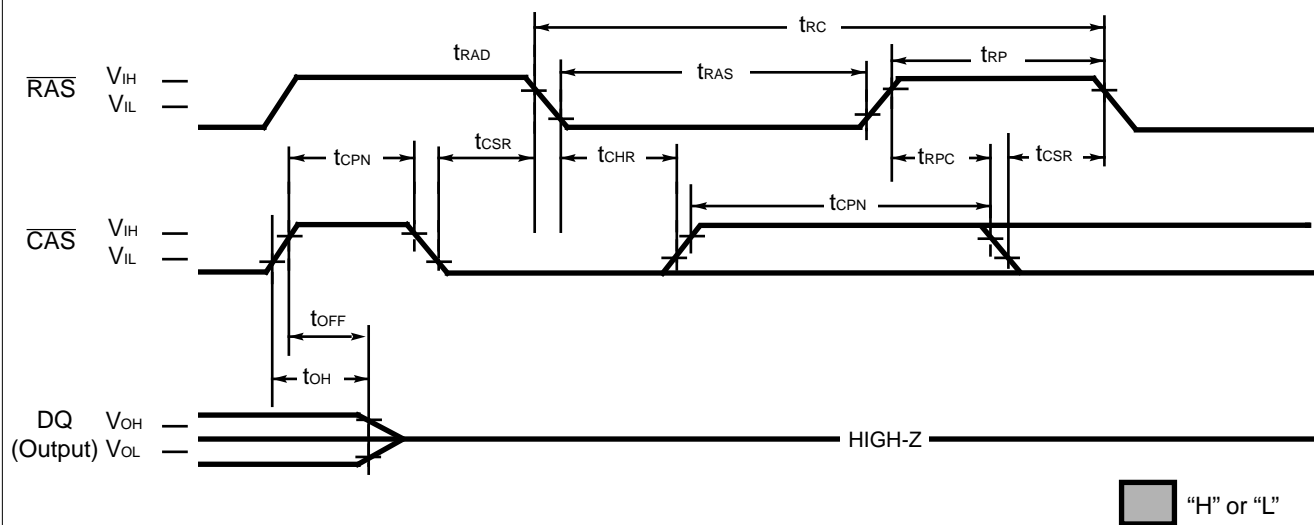


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 4096 row addresses every 65.6-milliseconds. Three refresh modes are available: $\overline{\text{RAS}}$ -only refresh, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, and hidden refresh.

$\overline{\text{RAS}}$ -only refresh is performed by keeping $\overline{\text{RAS}}$ Low and $\overline{\text{CAS}}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{\text{RAS}}$. During $\overline{\text{RAS}}$ -only refresh, D_{OUT} pin is kept in a high-impedance state.

Fig. 16 - $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH (ADDRESS = $\overline{\text{WE}} = \overline{\text{OE}} = \text{"H"}$ or "L")



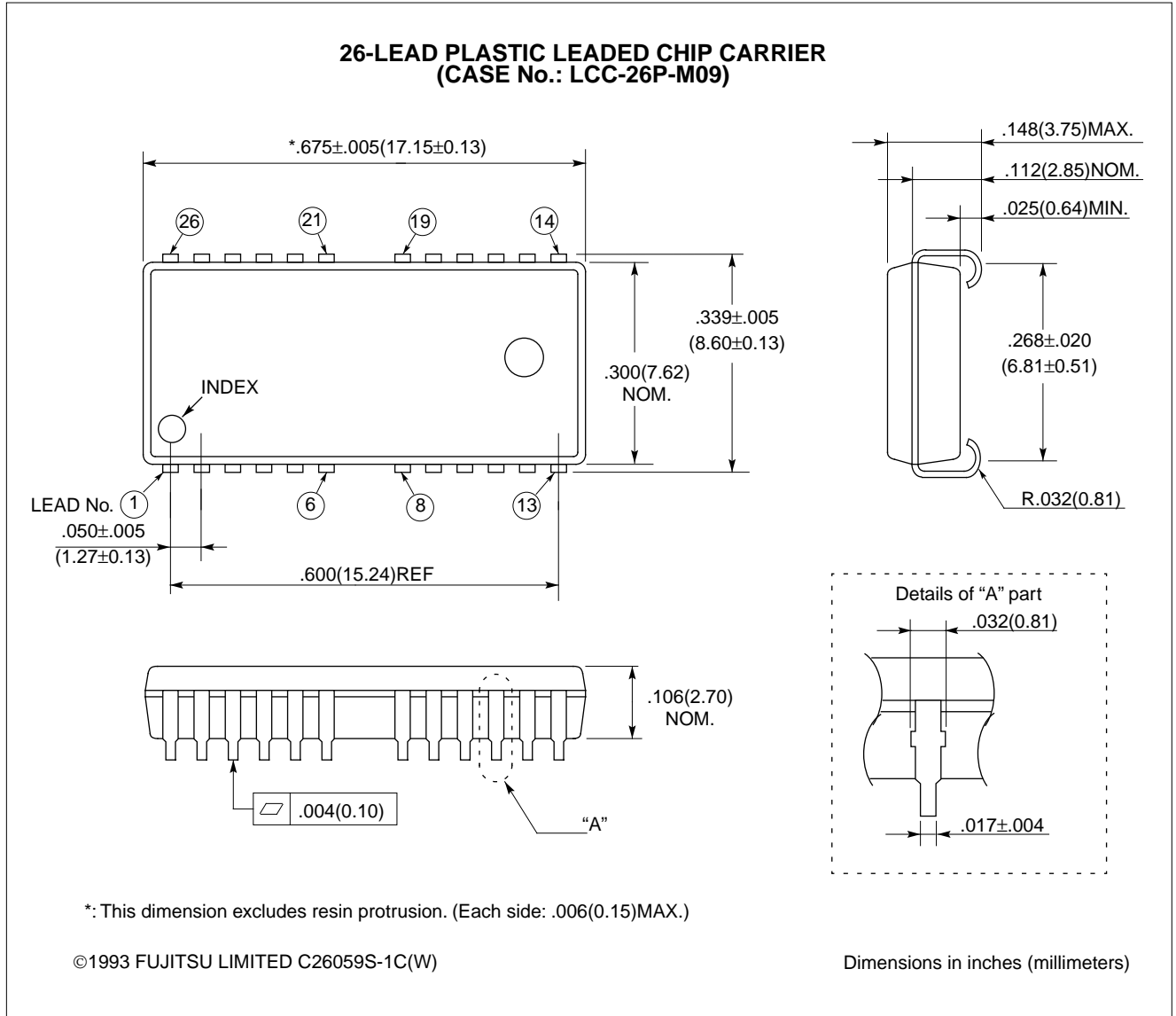
DESCRIPTION

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CAS}}$ is held Low for the specified setup time (t_{CSR}) before $\overline{\text{RAS}}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh operation.

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■ PACKAGE DIMENSIONS

(Suffix: -PJ)

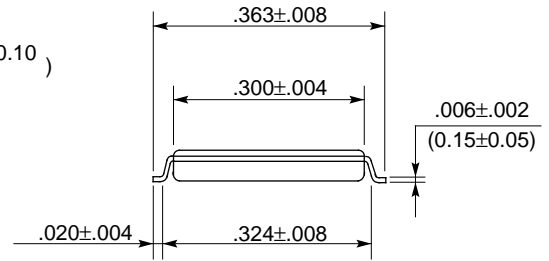
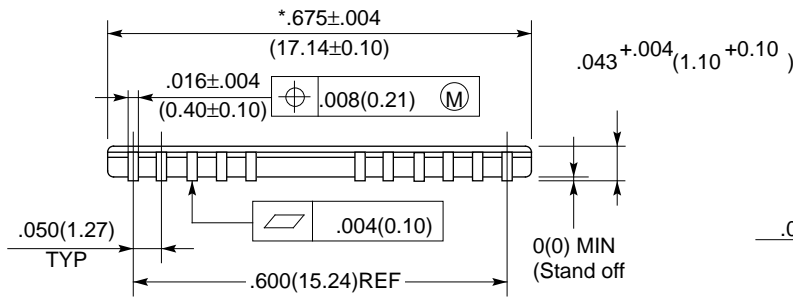
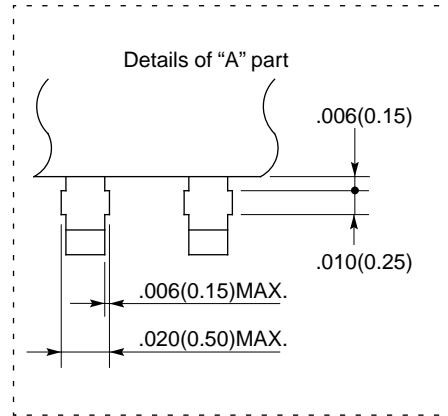
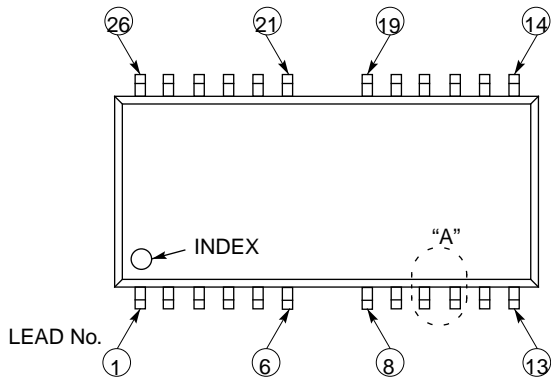


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■ PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTN)

26-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-26P-M05)



*: This dimension excludes resin protrusion. (Each side: $.006(0.15) \text{MAX.}$)

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Dimensions in inches (millimeters)

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